Microelectronics for Future RHIC Detectors

RHIC Detector Workshop – Nov. 13-14, 2001

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BNL

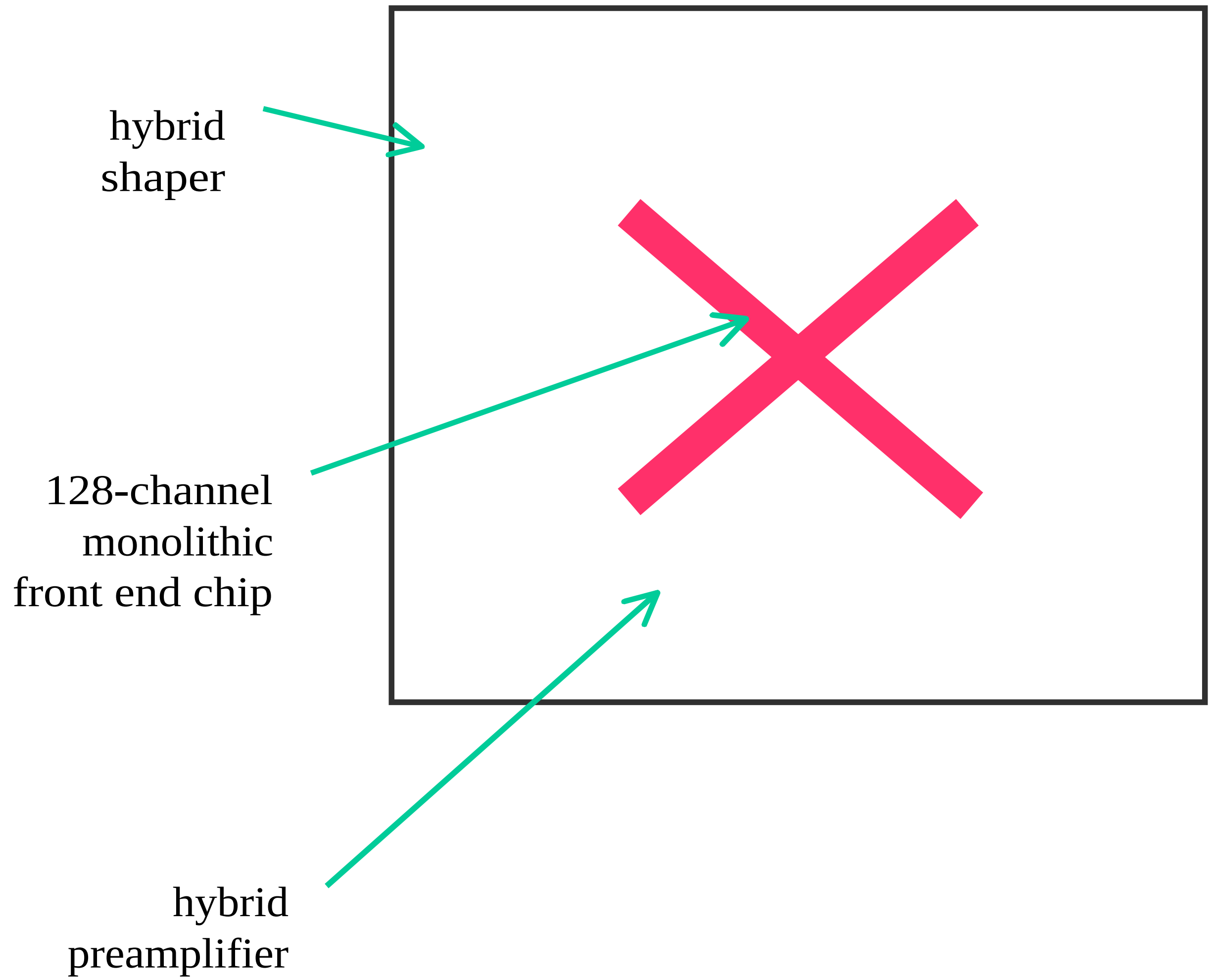
Outline

- Survey of present RHIC experiments
- Microelectronics Trends 1991 – 2001
  - CMOS scaling
  - Advances in packaging, PCB, assembly technology
- Power and Interconnect

Custom monolithic front ends

- Can be efficiently mass-produced with excellent economy of scale:
  - E.g., maskset + 10 wafers ~ $300K, 1000 chips/wafer
  - Additional wafer ~ $5K
  - Incremental cost < $10/chip
  - Chip may have 16 – 128 channels
- Can be located close to dense detector electrode arrays
  - pixels, micropattern & segmented cathode designs
- Can combine functions on single chip, replacing PCB/hybrid/cable connections with lower cost on-chip connection
- Can reduce power*

Advantages of monolithic realization



Improvement over hybrid + rack-based system:

Cost	X 200
Power:	X 10^3
Volume:	X $2*10^6$

Monolithic also adds functionality:

- *cal. pulse distribution*
- *sample/hold*
- *multiplexing*

Microelectronics in RHIC 2001

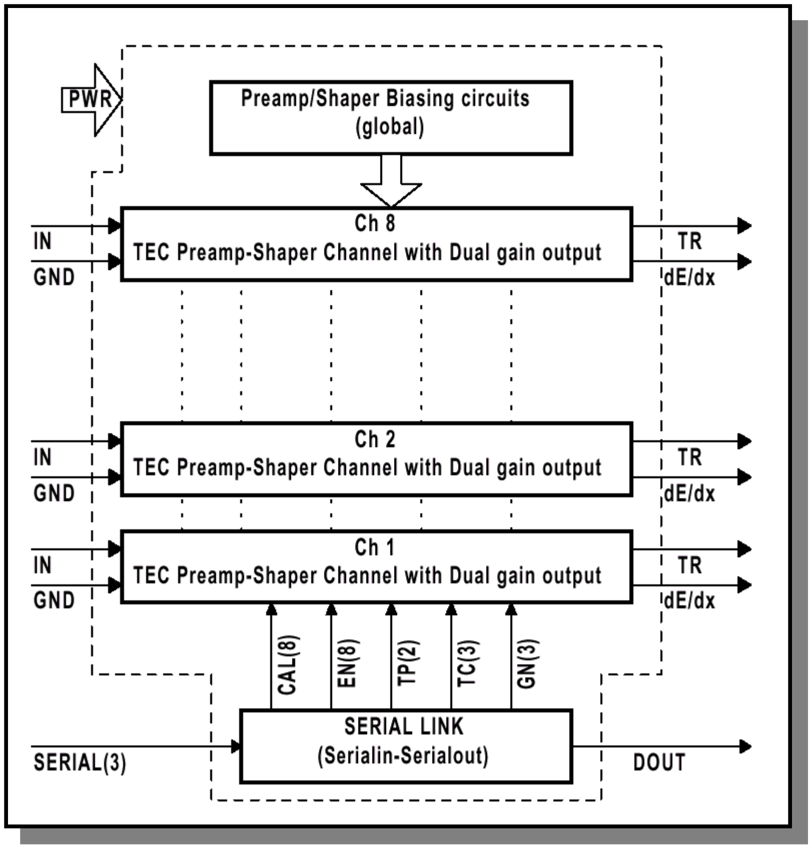
- STAR
  - TPC
    - CMOS 1.2 μm P/S, SCA, packaged
  - SVT
    - Bipolar P/S, CMOS 1.2 mm SCA, 240-channel ceramic hybrid
- PHENIX
  - MVD
    - 1.2 μm CMOS P/S, AMU/ADC, ceramic MCM
  - EMCAL
    - 1.2 μm CMOS integrator/VGA/TAC/sum, AMU/ADC, packaged
  - Pad chamber
    - 1.2 μm CMOS P/S/D, 1.0 μm CMOS DMU, packaged

Microelectronics in RHIC 2001 (con’t)

- PHENIX con’t.
  - Drift Chamber
    - Bipolar A/S/D, 0.8 μm CMOS TDC, packaged
  - Time Expansion Chamber
    - 1.2 μm CMOS P/S, FADC, 1.0 μm DMU packaged
  - RICH
    - 1.2 μm CMOS integrator/TAC, AMU/ADC, packaged
  - Muon tracker
    - 1.2 μm CMOS P/S, AMU/ADC packaged
- PHOBOS
  - Si pad
    - 1.2 μm CMOS (VA-HDR1 from IDE), chip-on-board

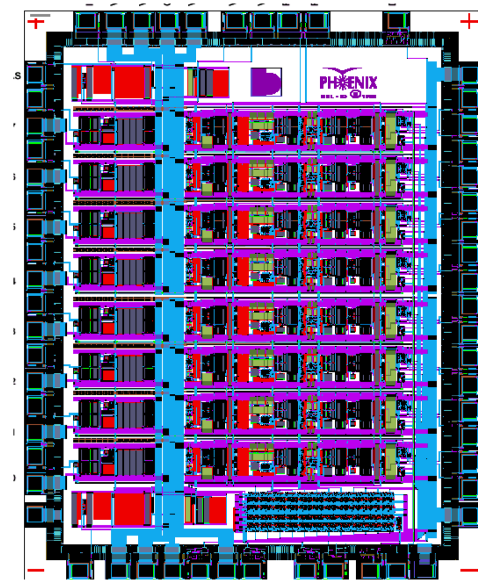
TEC-TRD Preamp/Shaper

Block Diagram

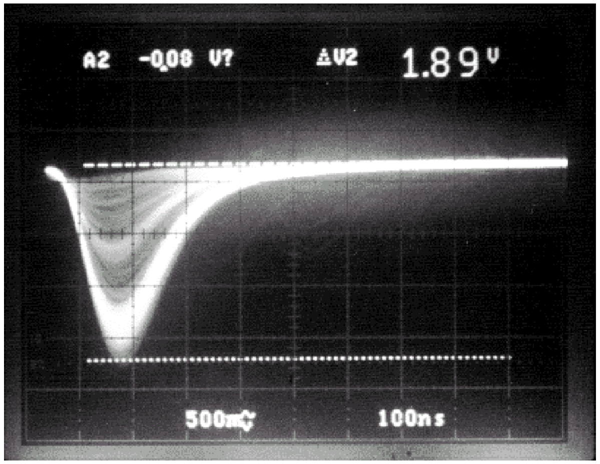


A. Kandasamy, E. O'Brien, P. O'Connor, W. VonAchen, "A monolithic preamplifier-shaper for measurement of energy loss and transition radiation" IEEE Trans. Nucl. Sci. 46(3), June 1999, 150-155

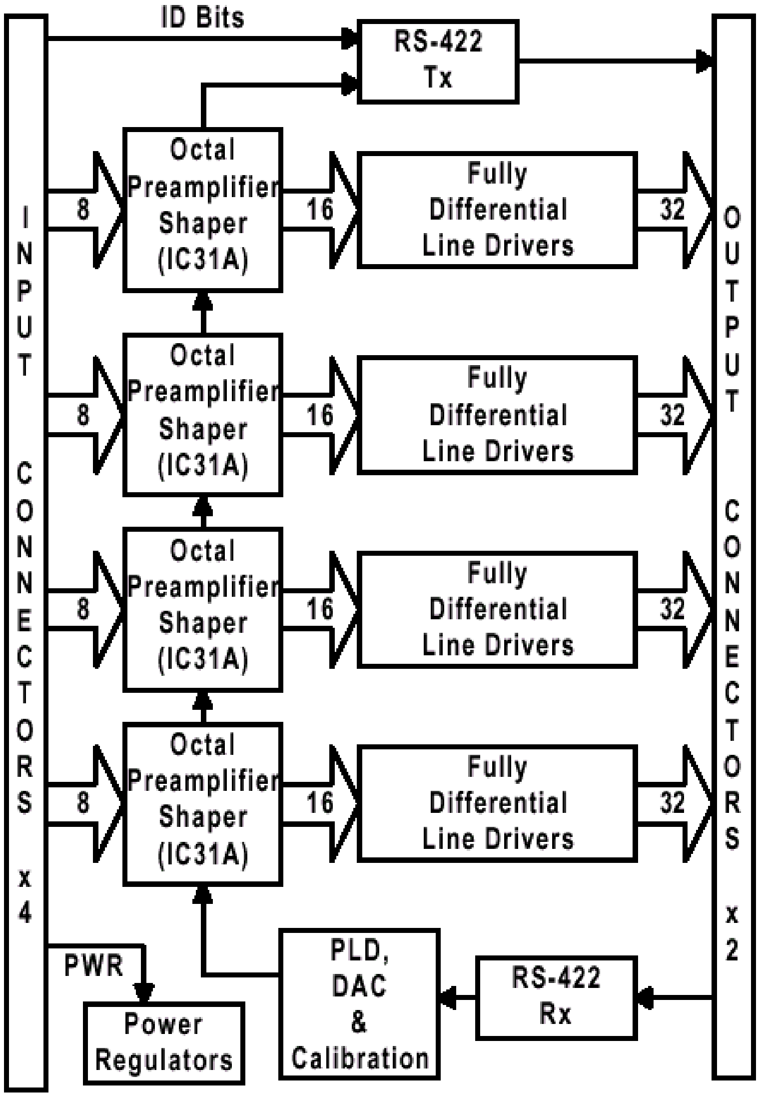
Die Layout

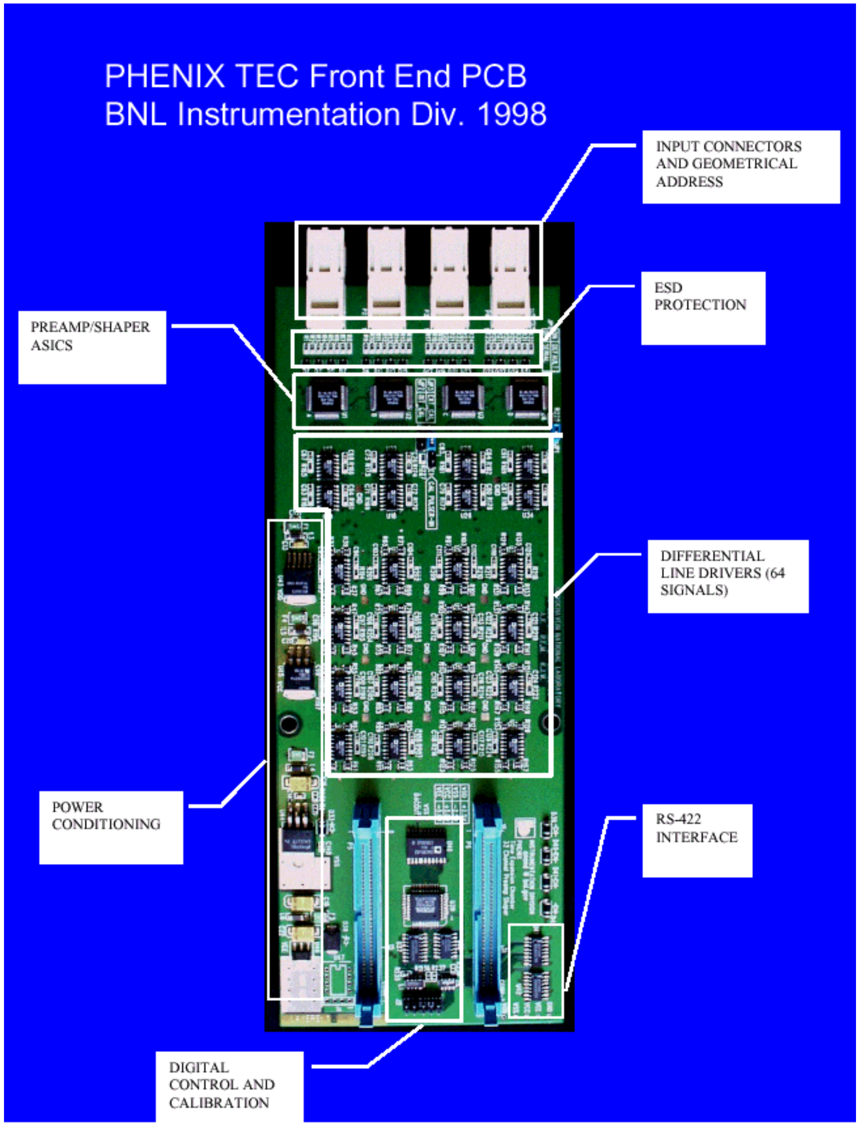


X-ray Response



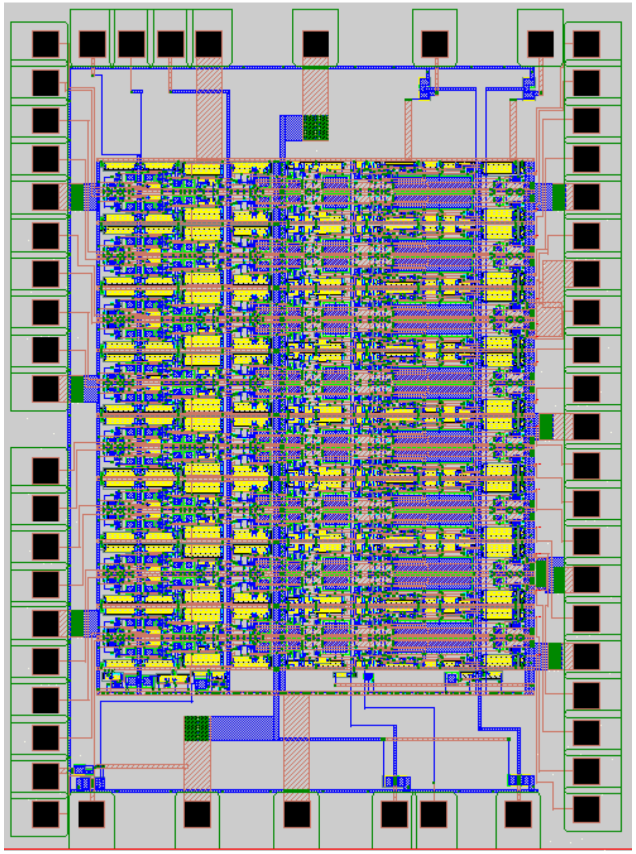
TEC Front-End Card



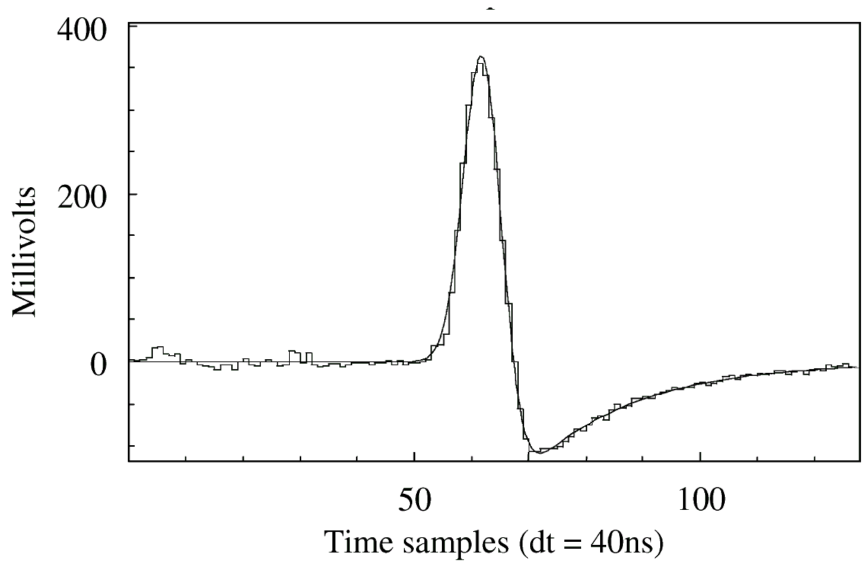


SVT Preamp/Shaper

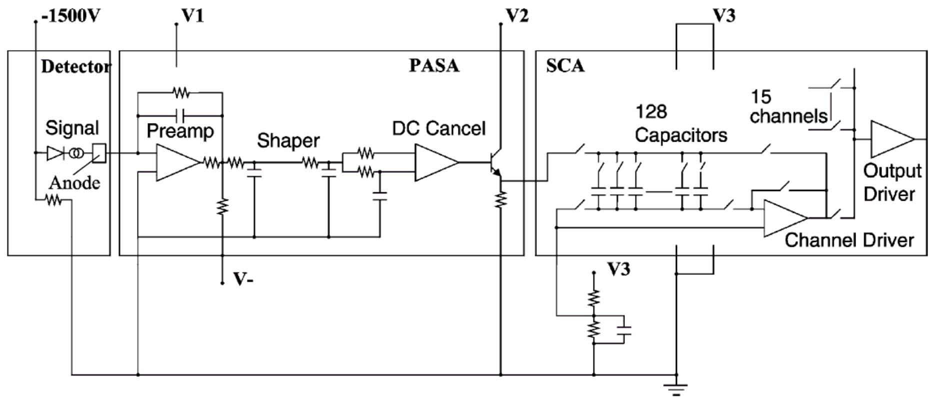
Die Layout

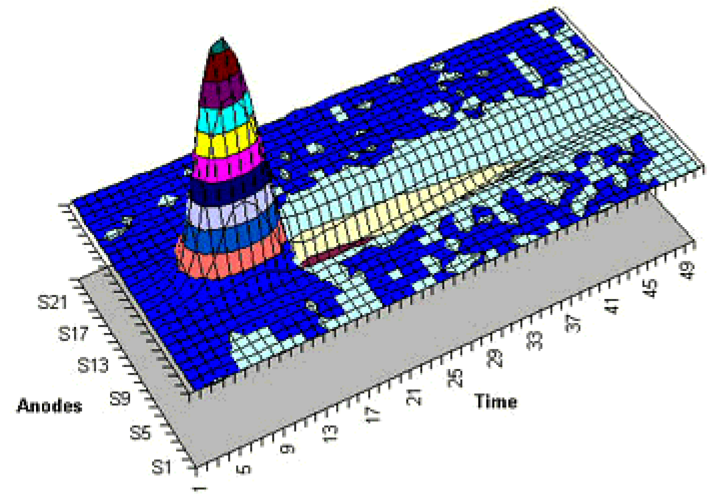


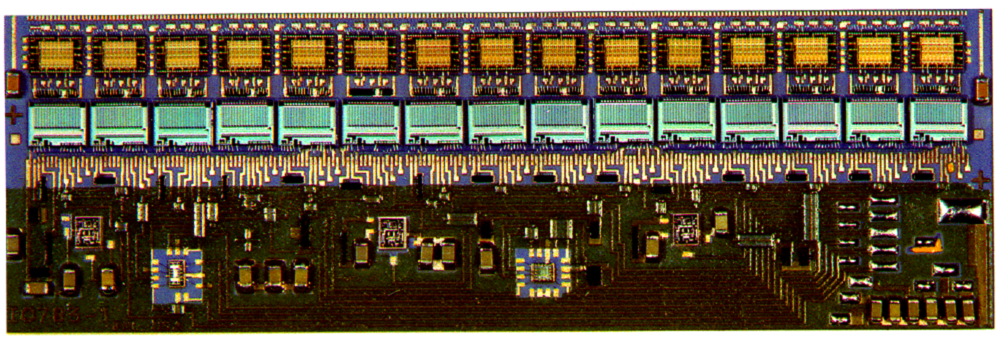
Output Waveform



SVT 240-channel multi-chip module







D. Lynn et al., "A 240 channel thick film multi-chip module for readout of silicon drift detectors", NIM A439 (2000), 418 - 426

Microelectronics in RHIC 2001 – Summary

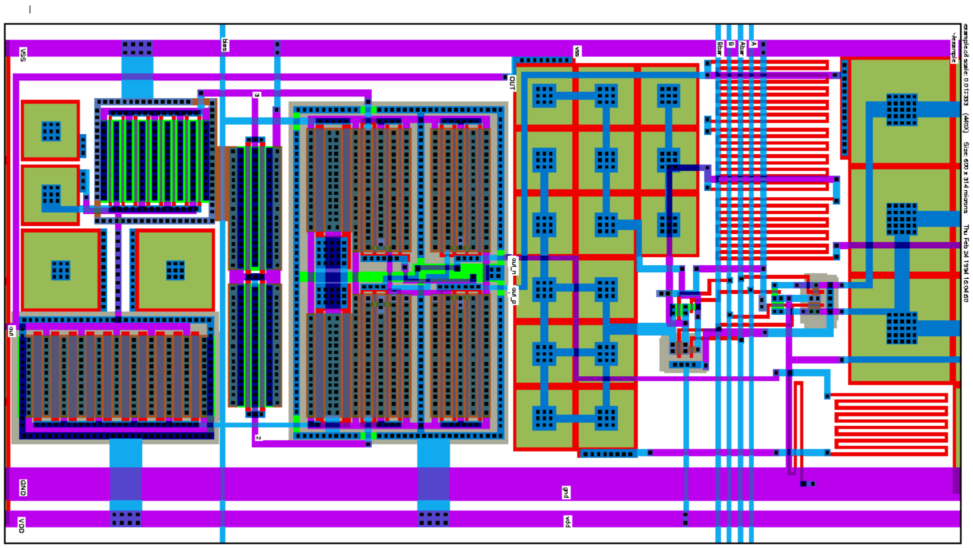
- Monolithics are used to read out all detector types:
  - Semiconductor
  - Gas avalanche
  - Scintillator/PMT
- About 0.5M channels instrumented with monolithic electronics
- About 17 custom chips have been developed
- Designs done by national laboratories (13), university groups (2), industry (3)

Custom Monolithics – technology options

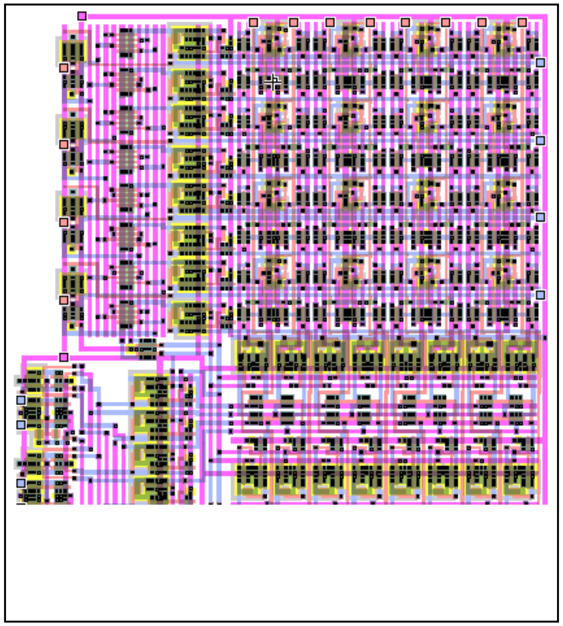
- Standard CMOS
  - Highest integration density
  - Suitable for most analog designs (low voltage issues for deep submicron)
  - Best for combining analog and digital
  - Widely available
  - Short life cycle (2 years/generation)
- Bipolar
  - Workhorse of “old” analog
  - Limited vendor availability
  - Speed/power advantage over CMOS (diminishing)
  - Low integration density
- BiCMOS
  - Complex process, expensive
- SiGe
  - Increasing use driven by RF circuits
  - Interesting for high frequency work
- Silicon on insulator (SOI)
  - Modest speed advantage for digital
  - Drawbacks for analog
  - Rad-hard
- GaAs
  - Digital, RF only

CMOS layout examples

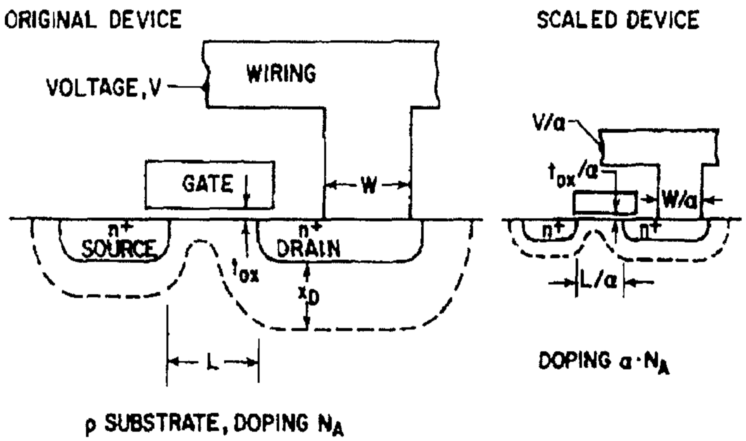
Analog

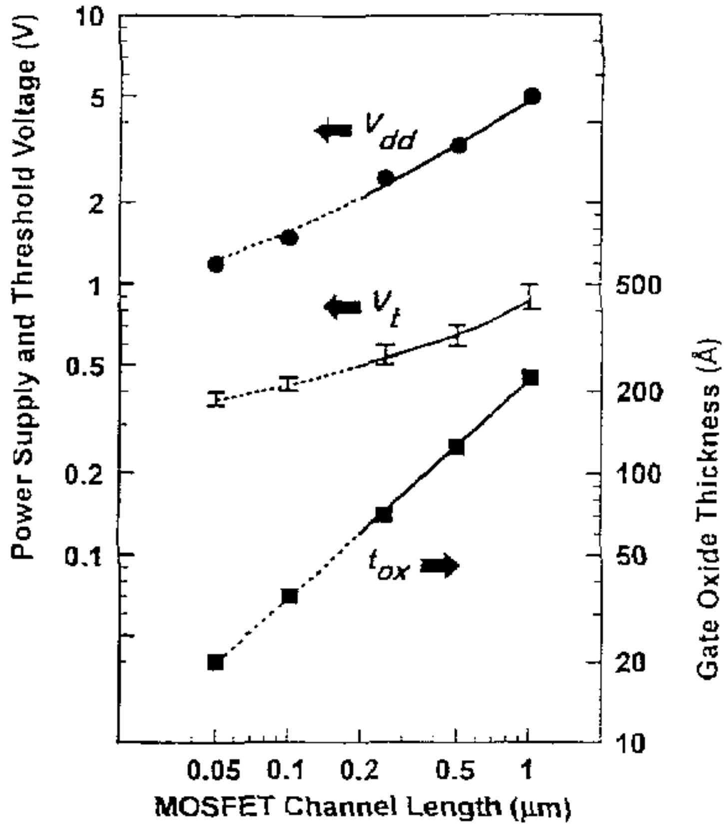


Digital



CMOS Scaling



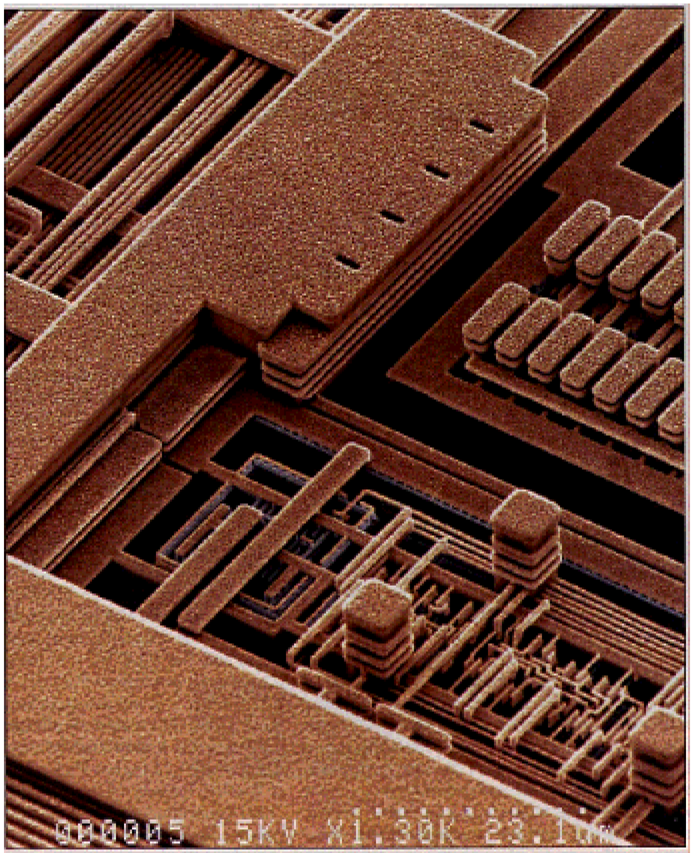


- Driven by digital VLSI circuit needs
- Goals: in each generation:
    - 2X increase in density
    - 1.5X increase in speed
    - Control short-channel effects, threshold fluctuation
    - < 1 failure in 10^7 hours

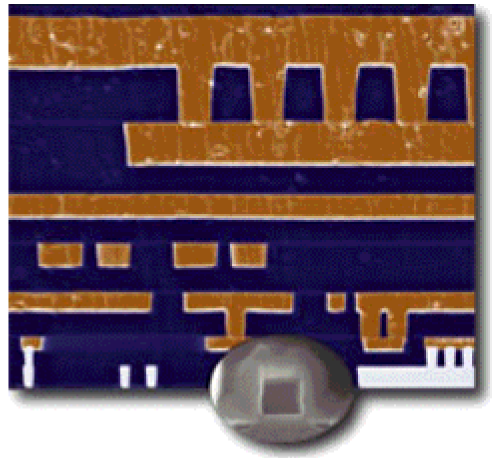
CMOS Technology Roadmap

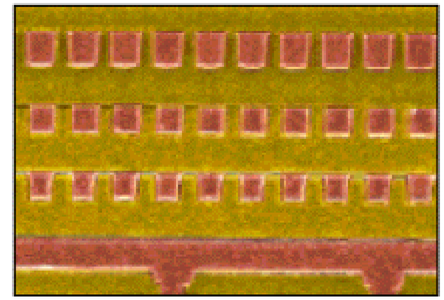
Year	**85**	**88**	**91**	**94**	**97**	**00**	**02**	**04**	**07**	**10**	**13**
Min. feature size [µm]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.10	0.07
Gate oxide [nm]	44	33	22	16	11	7.7	5.5	4.0	2.9	2.2	1.6
Power supply [V]	5	5	5	5	5/3.3	3.3	2.5	1.8	1.2	1	.7
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5	0.45	0.4	0.3	0.3	0.3

IBM Cu-11 Process (Blue Logic)



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].





Section showing Cu-11 copper and low-k dielectric process.

- L_{eff} =0.08 µm, L_{drawn} =0.11 µm
- Up to 40 million wireable gates
- Trench capacitor embedded DRAM with up to 16 Mb per macro
- Dense high-performance,comp lable SRAMs
- Power supply:1.2 V with 1.5 V opt on
- I/O power supply:3.3 V(dual oxide option)/
- 2.5 V(dual oxide option)/1.8 V/1.5 V
- Power dissipation of 0.009 µW/MHz/gate
- Gate delays of 27 picoseconds (2-input NAND gate)
- Seven levels of copper for global routing
- Low-k dielectric for high performance and reduced power and noise
- HyperBGA (flip chip):2577 total leads

Technology features for low-noise analog circuits

- High g_m/C_{gs} ratio (f_T)
- Low γ ($\gamma = g_m * R_n$)
- Low 1/f noise
- High input impedance device
- High g_m/g_d
- Controllable sub-nA current sources
- High-quality floating capacitor
- Good switch device
- Excellent AC isolation
- High supply voltage
- ESD-tolerant
- Radiation-tolerant

Color key:

improvement with scaling

no improvement expected

degradation with scaling

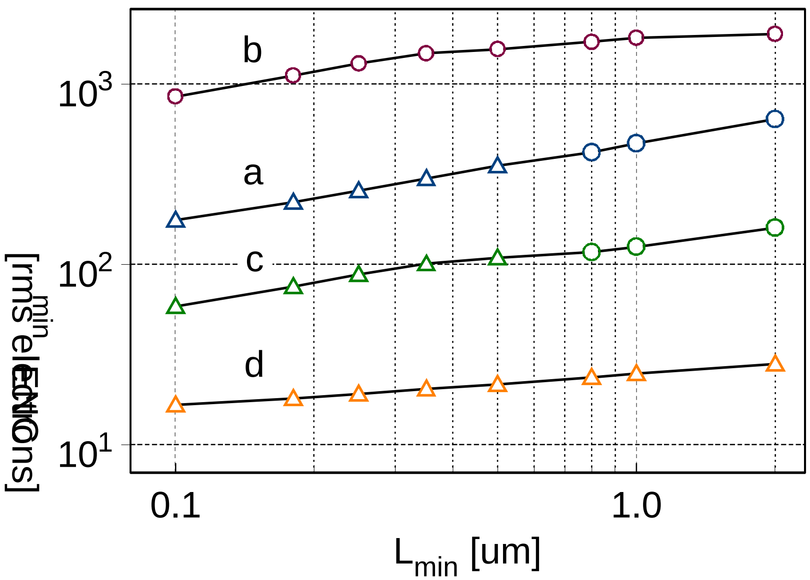
Noise and power vs. scaling

4 detector scenarios for scaling study

System	C_{det}	t_s	P	I_{leak}	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

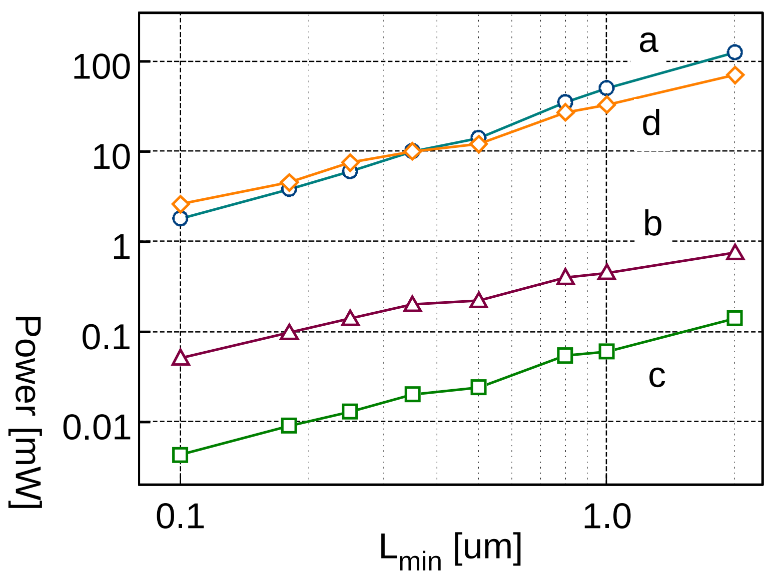
Noise vs. scaling

(power held constant)

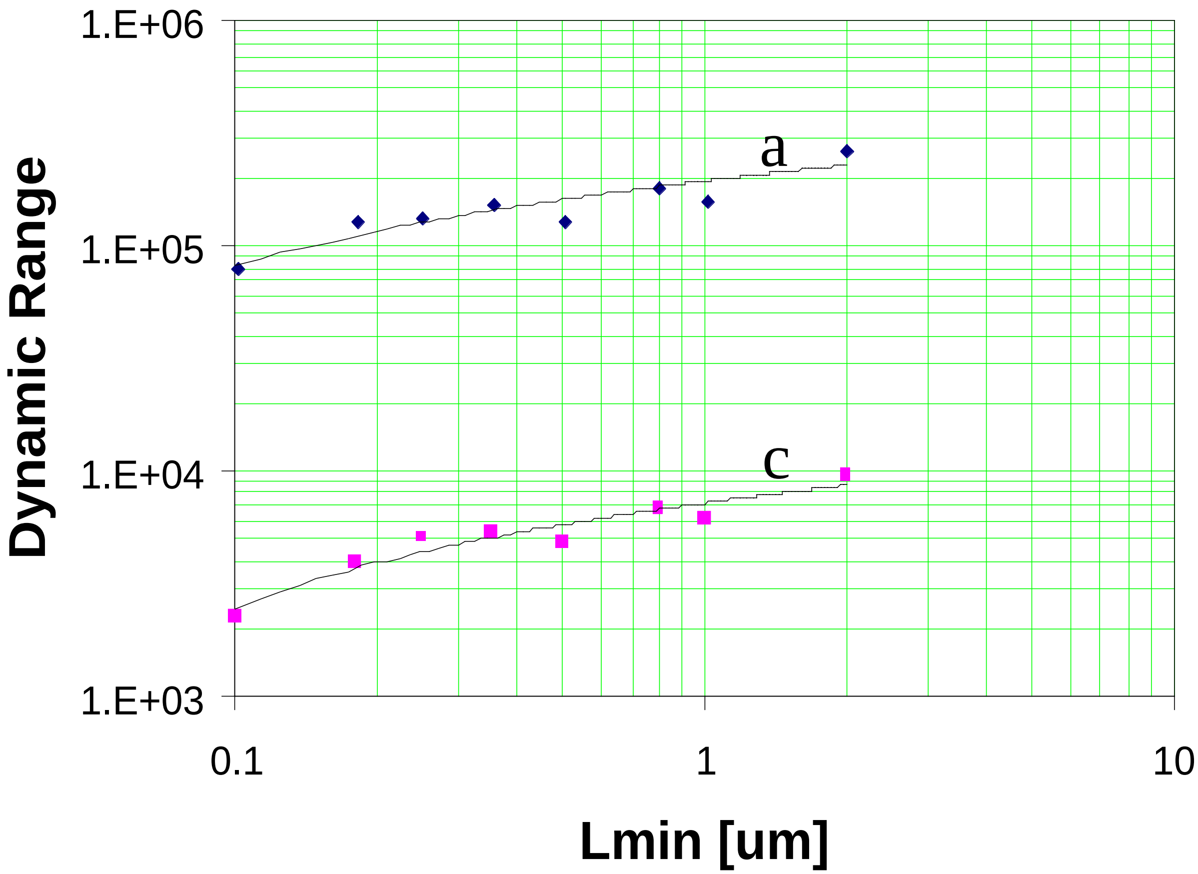


Power vs. scaling

(noise held constant)

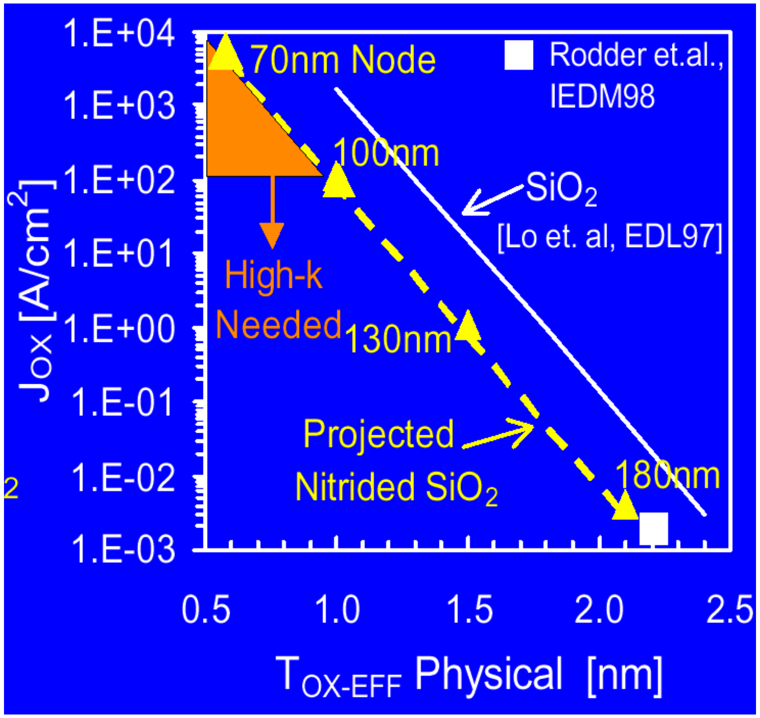


Dynamic range vs. scaling



Gate tunneling current

- Gate current expected to increase 100 – 200 x per generation below 0.18 μm
- J_{ox} ~ 100 A/cm^2 projected for L_{min} = 0.1 μm generation with nitrided SiO_2
- Considered tolerable for digital circuits (total gate area per chip ~ 0.1 cm^2)
- Typical CSA input FET would have I_G ~ 1 - 10 μA; ENCp ~ 2000 - 7000 rms e- at 1 μsec



SiO_2 gate leakage current (Lo et al., Electron Dev. Letters 1997)

Monolithics in scaled CMOS

- Analog:
  - Noise limits not changing significantly
  - Power can be reduced
  - Design effort required for high dynamic-range systems
  - Increased integration density, but not as much as digital
- Digital:
  - Big increase in integration density
  - Reduction in power
  - Big increase in clock frequency
  - Need to manage design complexity
- Analog/digital co-existence
  - Simulation capability limited
  - Anticipate the need to iterate

Power

Example: CMS Tracker

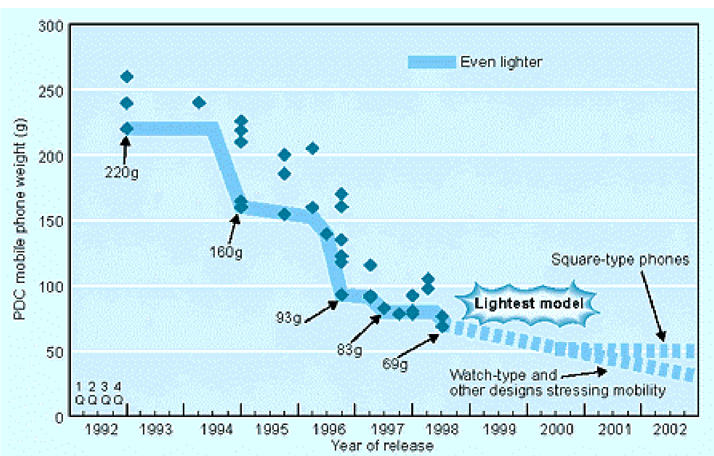
- Total # channels: 75,500 FE chips x 128 = ~10M
- Power/FE: 2.3 mW/channel
- Pwr/ch data TX: ~0.6 mW/channel
- Supply: 2.5 V and 1.25 V, P_{tot}= ~30 kW
- Total FE currents: IDD_{125}: ~7.5 kA, IDD_{250}: ~6.5 kA
- Remote supplies
- # of service cables: 1,800
- Power in the cables: > 75 kW
- Cross section of power cables and cooling pipes directly proportional to power dissipated !

Interconnect: Technology

- Significant advances in packaging, PCB, assembly technology
  - Thin- and fine-pitch leaded SMT components; BGAs; chip-scale packages; packages with low thermal resistance
  - Flip-chip and chip-on-board assembly
  - Microvias, thin-core laminates, flex for high density integration (HDI)
  - Passive component miniaturization, arrays

Cellular telephone handset trends

- 1991 cell phone
  - _ pound
  - 12V battery
  - 700 components
  - 8 hrs assembly time
  - $600
- 2001 cell phone
  - 2 oz.
  - 3V battery
  - 4 –5 modular components + passives integrated in substrate
  - 15 minute assembly time
  - < $150 or free



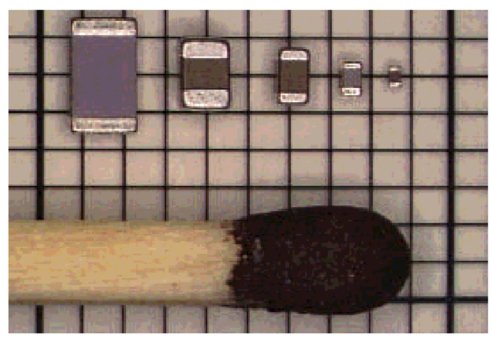
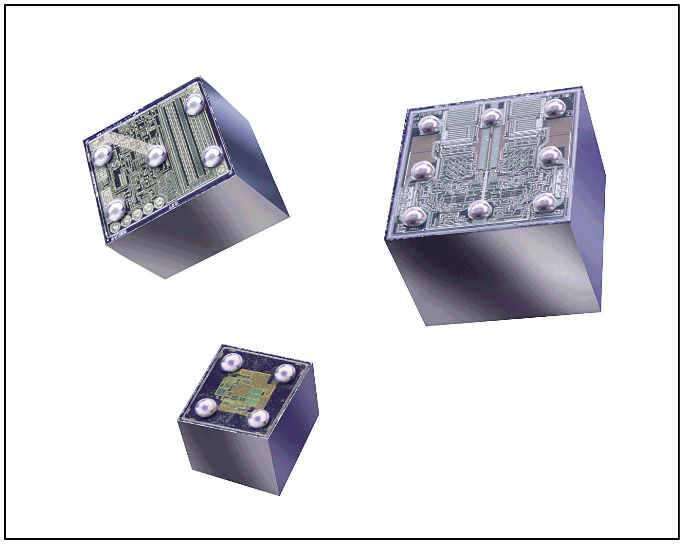


Figure 4 - Capacitors Ranging from 1206, 0805, 0603, 0402 and 0201

This is the world's first WRIST CAMERA. It features 1 MB of memory to hold up to 100 images.

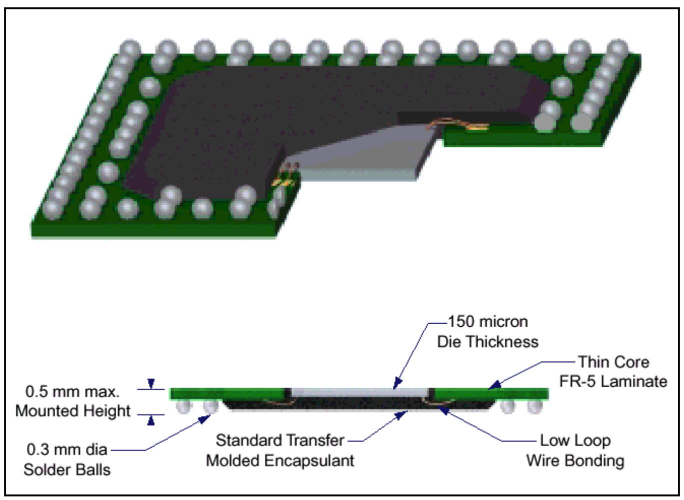
Standard packages of 2001



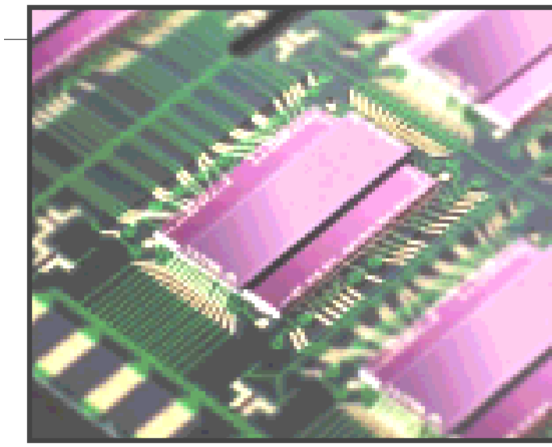
National microSMD

1.41 x 1.67 x 0.85mm body size (8L)

“Silicon Dust”



Amkor thin BGA



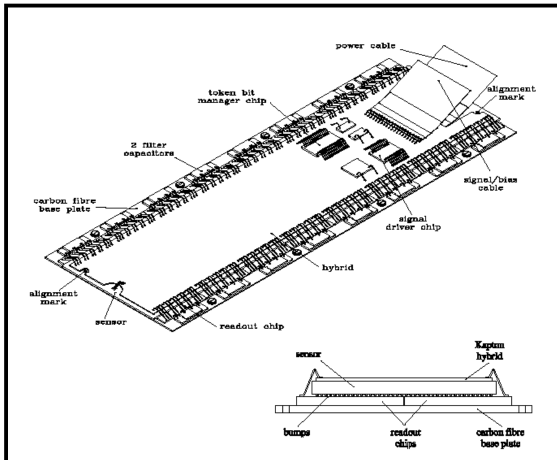
Stacked chip-scale package

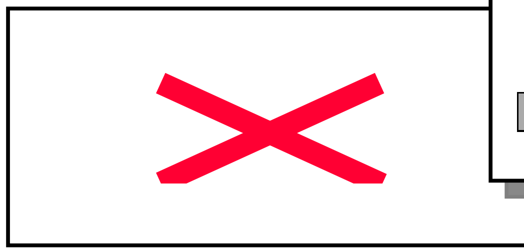
Interconnect issues in monolithic front ends

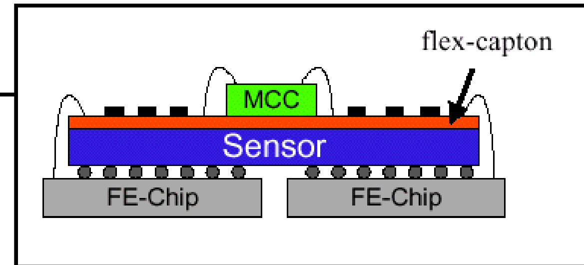
- Detector –> preamplifier
  - Lowest possible capacitance
  - Ease of assembly
  - Diagnostics
  - Repair/rework
- Front end –> ADC
  - Efficient use of expensive “analog” interconnect
- ADC –> off-detector processing
  - Efficient use of bandwidth for cost/power control
  - See:

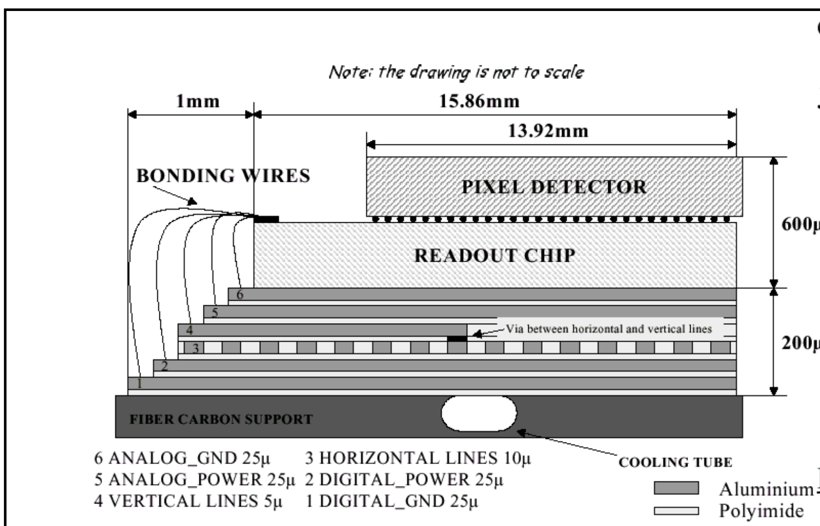
    http://snowmass2001.web.cern.ch/Snowmass2001/Docs/Marchioro%20Snowmass%202001.pdf
- System-level power distribution

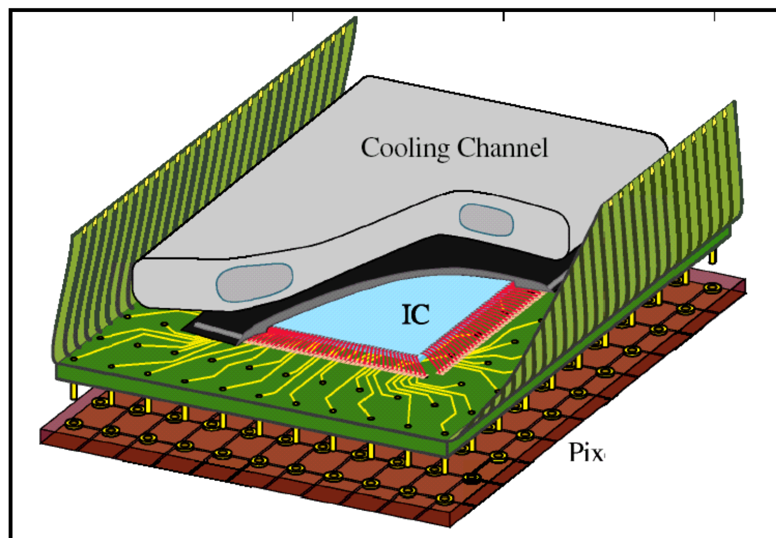
Detector-preamplifier connection can’t be designed after-the-fact!



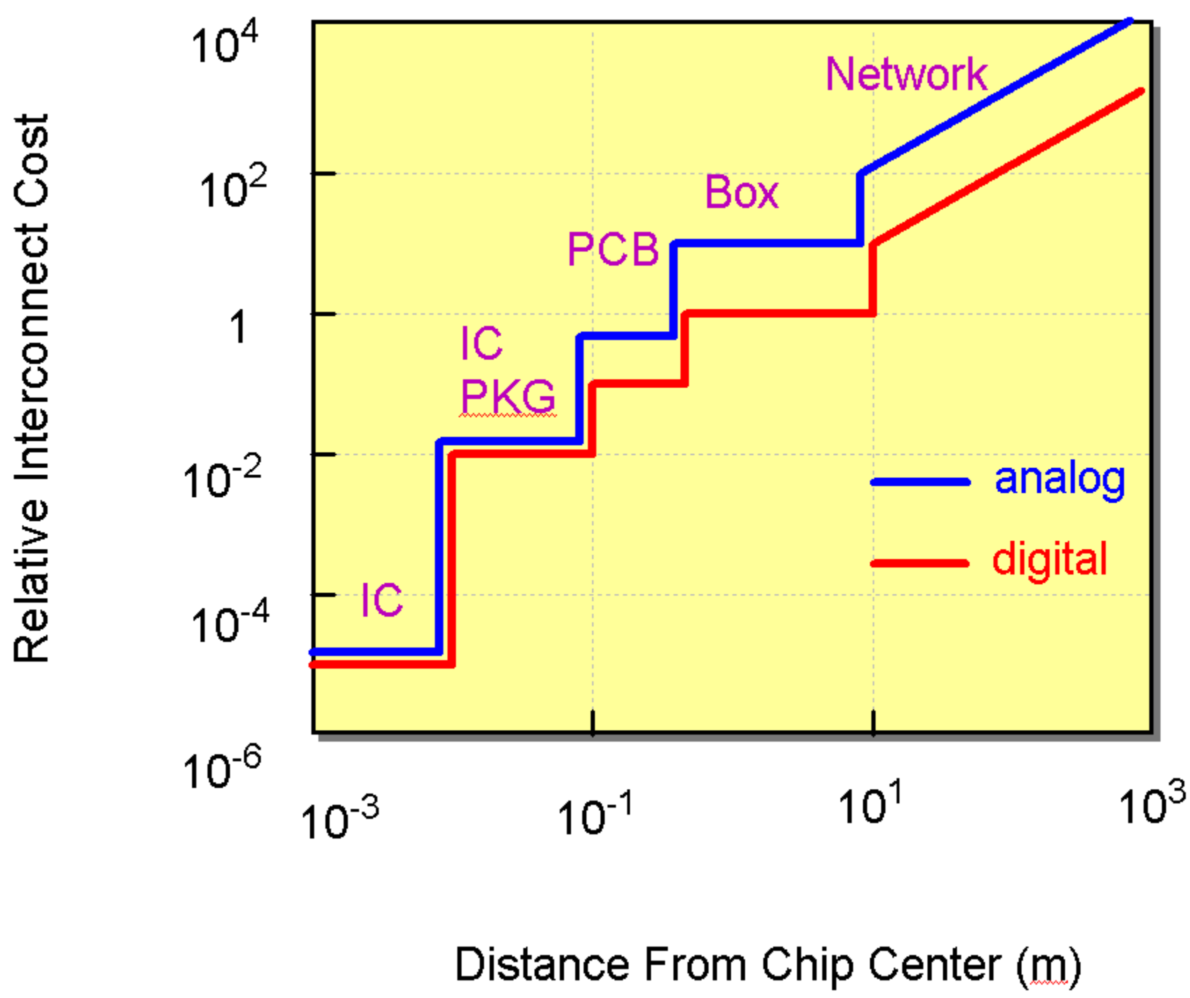








Cost of interconnect



ISSCC 2000

Summary

- RHIC detector upgrade programs can take advantage of a decade of progress in microelectronics.
- Up-front attention to power and interconnect issues is essential (avoid cable/connector/cooling problems after installation):
  - Look for opportunities to save power at all levels:
    - Technology
    - Circuit topology
    - Architecture
    - Algorithms
    - Data compression
  - For matrix-type detectors, design readout plane together with FEE
  - Maximize the use of on-chip interconnect
    - Don’t transfer analog data from chip-to-chip
    - Zero-suppress on-detector